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10/9/02

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:
Errol Todd Ryan

Serial No.: 09/706,043

Filed: November 3, 2000

For: Method for Forming Conductive Interconnects

Group Art Unit: 1765

Examiner: Vanessa Perez Ramos

Atty. Dkt. No.: 2000.060900

CERTIFICATE OF MAILING
37 C.F.R 1.8

I hereby certify that this correspondence is being deposited with the U.S. Postal Service with sufficient postage as First Class Mail in an envelope addressed to: Assistant Commissioner for Patents, Washington, D.C. 20231, on the date below:

9/30/02
Date

Signature

RESPONSE TO FIRST OFFICE ACTION DATED SEPTEMBER 9, 2002

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

This paper is submitted in response to the Office Action dated September 9, 2002 for which the shortened-statutory period for response is set to expire on December 9, 2002. Because this paper is being filed within the shortened statutory period for response, it is believed that no fees are due. Should, however, the Office require any extension of time and/or other fees deemed necessary for entry of this paper, please consider this paragraph such a request and authorization for the Assistant Commissioner to withdraw the appropriate fee under 37 C.F.R. §§ 1.16 to 1.21 from Williams, Morgan & Amerson, P.C. Deposit Account No.

50-0786/2000.060900. Reconsideration of the application in view of the following amendments and remarks is respectfully requested.

AMENDMENT

Please amend claim 45 as follows.

45. (Amended) A method for forming a conductive interconnect in a semiconductor device, comprising:

forming a first process layer above a semiconductor substrate;

forming a second process layer above the first process layer;

A1 forming a mask above the second process layer, the mask having an opening therein;

performing a first anisotropic etch into a region of the second process layer underlying the opening in the mask, leaving a portion of the second process layer in the etched region;

removing the mask from above the second process layer;

performing a second anisotropic etch to form an opening in the first process layer; and

forming a conductive material in the opening in the first process layer.